Remarks

Claims 23-25, 27-31, 34, and 35 are currently pending in this application.

The Office Action objected to the drawings as failing to show reference numeral "17"; rejected claims 23-25 and 27-29 under 35 U.S.C. § 103(a) as being unpatentable over Deleonibus (U.S. Patent No. 6,091,076) in view of Koh (U.S. Patent No. 6,049,110); rejected claims 23-25 and 27-31 under 35 U.S.C. § 103(a) as being unpatentable over Yamaguchi et al. (U.S. Patent No. 5,341,028) in view of Imai (U.S. Patent No. 6,297,529) and Koh; rejected claim 34 under 35 U.S.C. § 103(a) as being unpatentable over Yamaguchi et al. in view of Gardner et al. (U.S. Patent No. 6,096,615) and Koh; rejected claim 35 under 35 U.S.C. § 103(a) as being unpatentable over Yamaguchi et al. in view of Gardner et al. and Koh, and further in view of Imai; rejected claim 34 under 35 U.S.C. § 103(a) as being unpatentable over Deleonibus in view of Gardner et al. and Koh; and rejected claim 35 under 35 U.S.C. § 103(a) as being unpatentable over Deleonibus in view of Gardner et al. and Koh, and further in view of Imai.

By this Amendment, Applicants have corrected the informalities noted by the Office Action in the drawings, and respectfully request withdrawal of the objection to the drawings.

The present invention recited in, for example, claim 23, and claims 24, 25, and 27-31 at least by virtue of dependence, comprises a combination of elements, including extension regions arranged in the semiconductor layer on both sides of the gate conductor and extending under and contacting the spacers and a portion of the gate conductor, wherein a portion of at least one of the extension regions is exposed at a surface of the semiconductor layer by removing at least a part of one of the spacers; and a metal layer formed at least in the exposed portion of the extension region, the metal layer contacting the semiconductor layer and the exposed portion of the extension region.

Deleonibus discloses a MOS transistor having extension regions 8, 10 (as defined by the Office Action), however the extension regions are not formed in a semiconductor layer. In fact, Deleonibus fails to disclose a semiconductor layer at all. Thus, the reference fails to disclose that the extension regions 8, 10 contact the gate conductor 20 and the spacers 24, 26, and that at least one extension region is exposed at the surface of the semiconductor layer (not present in Deleonibus). Deleonibus also discloses a metal layer 12, 14 (as defined by the Office Action), but the metal layer does not contact a semiconductor layer (due to its nonexistence) and does not contact the exposed portion of the extension region because the reference fails to disclose such an exposed portion.

Koh discloses a MOS transistor but fails to disclose extension regions that contact a gate conductor 56 and spacers 55, and that at least one extension region is exposed at the surface of the semiconductor layer (not present in Koh). It is not clear from Fig. 43 of Koh whether regions 43 contact gate conductor 56 and spacers 55. Koh also fails to disclose a metal layer that contacts a semiconductor layer (due to its nonexistence) and contacts the exposed portion of the extension region because the reference fails to disclose such an exposed portion.

Therefore, Deleonibus and Koh, whether taken alone or in any reasonable combination, fail to disclose or suggest the combination of elements recited in claims 23-25 and 27-31, including extension regions arranged in the semiconductor layer on both sides of the gate conductor and extending under and contacting the spacers and a portion of the gate conductor, wherein a portion of at least one of the extension regions is exposed at a surface of the semiconductor layer by removing at least a part of one of the spacers; and a metal layer formed at least in the exposed portion of the extension region, the metal layer contacting the semiconductor layer and the exposed portion of the extension region.

Yamaguchi et al. disclose a semiconductor device having extension regions 15, 16 (as defined by the Office Action), however the extension regions are not formed in a semiconductor layer. In fact, Yamaguchi et al. fail to disclose a semiconductor layer at all. Thus, the reference fails to disclose that the extension regions 15, 16 contact the gate conductor 20 and the spacers 25, 26, and that at least one extension region is exposed at the surface of the semiconductor layer (not present in Yamaguchi et al.). Yamaguchi et al. also disclose a metal layer 27 (as defined by the Office Action), but the metal layer does not contact a semiconductor layer (due to its nonexistence) and does not contact the exposed portion of the extension region because the reference fails to disclose such an exposed portion.

Imai fails to disclose extension regions 16 that contact a gate conductor 14 and spacers 17, and that at least on extension region is exposed at the surface of a semiconductor layer. Imai also fails to disclose that a metal layer 20 contacts the semiconductor layer and the exposed portion of the extension region because the reference fails to disclose such an exposed portion. Note that metal layer 20 of Imai (Fig. 2) is located at the top of gate conductor 14.

Koh fails to disclose extension regions that contact a gate conductor 56 and spacers 55, and that at least one extension region is exposed at the surface of the semiconductor layer (not present in Koh). Koh also fails to disclose a metal layer that contacts a semiconductor layer (due to its nonexistence) and contacts the exposed portion of the extension region because the reference fails to disclose such an exposed portion.

Therefore, Deleonibus, Imai, and Koh, whether taken alone or in any reasonable combination, fail to disclose or suggest the combination of elements recited in claims 23-25 and 27-31, including extension regions arranged in the semiconductor layer on both sides of the gate conductor and

extending under and contacting the spacers and a portion of the gate conductor, wherein a portion of at least one of the extension regions is exposed at a surface of the semiconductor layer by removing at least a part of one of the spacers; and a metal layer formed at least in the exposed portion of the extension region, the metal layer contacting the semiconductor layer and the exposed portion of the extension region.

The present invention recited in, for example, claim 34, and claim 35 at least by virtue of dependence, comprises a combination of elements, including extension regions provided under and contacting the first and second sidewall spacers, the extension regions contacting the gate and extending further under the gate than the source and drain diffusion regions, wherein a portion of at least one of the extension regions is exposed at a surface of the body region by removing at least a part of one of the first and second sidewall spacers; and a conductor formed at least in the exposed portion of the extension region, the conductor being in contact with the exposed portion of the extension region and at least a portion of the source diffusion region to form a Schottky diode.

As discussed above for claims 23-25 and 27-31, Deleonibus, Koh, Yamaguchi et al. and Imai fail to disclose the very elements highlighted in claims 34 and 35. Gardner was cited by the Office Action for the disclosure of a first sidewall spacer that is thinner than a second sidewall spacer. Gardner, however, fails to disclose extension regions contacting the gate and the spacers, a portion of one extension region being exposed at a surface of the body region, and a conductor in contact with exposed portion of the extension region at a portion of the source diffusion region.

Therefore, Deleonibus, Koh, Yamaguchi et al., Imai, and Gardner, whether taken alone or in any reasonable combination, fail to disclose or suggest the elements recited in claims 34 and 35, including extension regions provided under and contacting the first and second sidewall spacers, the

extension regions contacting the gate and extending further under the gate than the source and drain diffusion regions, wherein a portion of at least one of the extension regions is exposed at a surface of the body region by removing at least a part of one of the first and second sidewall spacers; and a conductor formed at least in the exposed portion of the extension region, the conductor being in contact with the exposed portion of the extension region and at least a portion of the source diffusion region to form a Schottky diode.

In light of the above, Applicants submit that none of the prior art references applied against this application, whether taken alone or in any reasonable combination, discloses or suggests the combination of elements recited in claims 23-25, 27-31, 34, and 35. Thus, these claims are allowable over these references. Applicants, therefore, respectfully request the reconsideration and withdrawal of the Section 103(a) rejections of these claims. Applicants further request reconsideration of the application, and the timely allowance of the pending claims.

If there are any other fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 03-2775. If a fee is required for an extension of time under 37 C.F.R. § 1.136 not accounted for above, such an extension is requested and the fee should also be charged to our Deposit Account.

Respectfully submitted,

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